REMARKS

Amendment to the Claims

Applicant has amended claim 47 to correct a typographical error in that claim 47 now depends from claim 42 rather than claim 37. Thus, as set forth in the Office Action, claim 47 would now be in Group I instead of Group VI.

Applicant has also amended the preambles of claims 1-8, 17-24 and 33-34 to clarify the claimed inventions.

Applicant's Election If Election/Restriction Not Withdrawn in Response to Traverse Below

If the election/restriction is not withdrawn or modified in response to the traverse below, Applicant makes the following election – Group VI. This group includes claims 35-41.

Traverse of Election/Restriction Requirement

In setting forth the election/restriction requirement, the Office Action set forth six different claim groupings. In so doing, the Office Action relies upon MPEP 806.05(c) and 806.05(d).

Applicant respectfully asserts that the Office Action incorrectly applies these provisions of the MPEP to the current claims. The current apparatus claims (claims 1-41) and the current method claims 42-63) are structured as follows:

• Claim 33 -	array	+	receive module	+	transmit module
• Claim 35 -			receive module	+	transmit module
• Claim 1 -	array	+	receive module		
• Claim 9 -			receive module		
• Claim 17 -	array			+	transmit module
• Claim 25 -					transmit module
• Claim 42 -	array	+	receiving signals		
• Claim 48 -			receiving signals		
• Claim 53 -	array			+	transmitting signals
• Claim 59 -					transmitting signals

Applicant respectfully asserts that the claims should be properly considered as claims to $AB_{specific}/B_{specific}$ under MPEP 806.05(c)II, for which an election/restriction is not proper. In particular, the following pairs of claims clearly fall within this provision and should not be restricted: (1) claims 33 and 35, (2) claims 1 and 9, (3) claims 17 and 25, (4) claims 42 and 48, and (5) claims 53 and 59.

In addition, as partially recognized in the Office Action, the method claims should not be restricted from the correlating apparatus claims, as set forth in MPEP 806.05(e). Thus, the following pairs of claims should not be restricted: (1) claims 1 and 42, (2) claims 9 and 48, (3) claims 17 and 53, and (4) claims 25 and 59. (NOTE – The Office Action included claims 59-63 in Group III; however, these claims are more properly placed in the Action's Group IV.)

In summary, based upon these two clear rules from the MPEP, the only claim groupings that should be argued to be properly restricted are the following:

- NEW GROUP I – Claims 1-16 and 42-52 (receiver claims)
- NEW GROUP II – Claims 17-32 and 53-63 (transmitter claims)
- NEW GROUP III – Claims 33-41 (transceiver claims that combine limitations from the receiver claims and the transmitter claims)

Even assuming these new claim groupings were made, however, Applicant respectfully asserts that **all the claims should be considered together** for the following reasons:

- **Patentability Is Related** – The pending claims distinguish from prior art systems in a similar way. Rather than use the prior art method of adjusting the outputs of the ADC and DAC with a programmable delay, as shown in FIG. 1 (Prior Art), the claims require that the sampling clock 110 that drives the ADC 108 in the receive path circuitry and DAC 112 in the transmit path circuitry be adjusted by a programmable time delay 208. [See FIGS. 3A-3C and associated text.] Thus, the outputs of the ADC 108 and DAC 112 themselves are directly controlled through the programmable delay adjustments to the clock signals for the ADC 108 and DAC 112. [See Application page 12, lines 11-18.]

- **Separate Searches Not Required** – In examining NEW GROUP III (or in just examining Group VI as set forth in the Office Action), the Examiner would cover both the receiver limitations and the transmitter limitations. Thus, there would not be a need for a separate search, thereby negating the primary argument for restricting the claims.

- **Linking Claims Exist** – Claims 33 and 35 should be considered linking claims within MPEP 809 and 809.03. Under this provision, the other groups could be provisional restricted;

however, if these claims were allowed, the restriction of the other claims would have to be lifted.

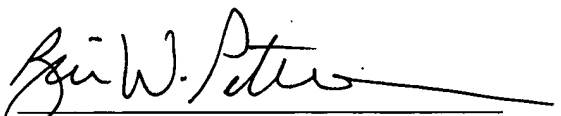
- **Similar Claim Configuration Examined Together and Given Positive IPER in the PCT Examination** – The EPO examined together claims that included independent claims directed to the following: (1) a digital phased array receiver, (2) a digital phase array transmitter, (3) a digital phased array transmit/receive module, (4) a method for receiving signals, and (5) a method for transmitting signals. For the Examiner's convenience, a copy of the amended claims that were examined and a copy of the IPER are enclosed.

Conclusion

Applicant respectfully requests reconsideration of the restriction requirement. In particular, Applicant respectfully requests that the restriction requirement be completely withdrawn. Or in the alternative, Applicant respectfully requests that claims 33 and 35 be considered linking claims, that these claims be fully examined together, and that upon allowance of these claims, any restriction of the other claims be withdrawn, as required by MPEP 809.

The Examiner is invited to contact the undersigned at the phone number indicated below with any questions or comments or to otherwise facilitate expeditious and compact prosecution of the application.

Respectfully submitted,



Brian W. Peterman
Registration No. 37,908
Attorney for Applicant

O'KEEFE, EGAN & PETERMAN
1101 Capital of Texas Highway South
Building C, Suite 200
Austin, Texas 78746
(512) 347-1611
FAX: (512) 347-1615

Claims

We claim:

1. A digital phased array receiver for receiving electromagnetic energy, comprising:

a plurality of antenna elements capable of receiving electromagnetic energy; and

a receive module coupled to each of the plurality of antenna elements, the receive module including an analog to digital converter controlled by a clock signal generated by clock circuitry coupled to a delay circuit;

wherein each delay circuit delays a base clock signal from the clock circuitry by a desired amount so that a receive direction of the plurality of antenna elements may be electronically controlled.

2. The digital phased array receiver of claim 1, wherein each analog to digital converter has a multiple bit digital value as an output.

3. The digital phased array receiver of claim 1, wherein each analog to digital converter has a single bit digital value as an output.

4. The digital phased array receiver of claim 1, further comprising multiple data conversion circuits coupled to receive the output of each analog to digital converter at a first clock rate and having an output signal at a second clock rate.

5. The digital phased array receiver of claim 4, wherein the first clock rate matches the base clock signal and the second clock rate is slower than the first clock rate.

6. The digital phased array receiver of claim 1, wherein an amount of delay provided by each delay circuit is programmable.

7. The digital phased array receiver of claim 6, wherein the plurality of antenna elements are grouped into sets of antenna elements and wherein each antenna element within the same set has the same amount of programmed delay.

8. The digital phased array receiver of claim 1, wherein the electromagnetic energy is radio-frequency energy.

9. The digital phased array receiver of claim 6, wherein each delay circuit is controlled by a digital word provided by a control register that may be loaded with a desired delay value.

10. The digital phased array receiver of claim 1, further comprising synchronization circuitry coupled to each analog to digital converter to receive and then output data from the analog to digital converter at an output clock rate.

11. The digital phased array receiver of claim 14, wherein for each receive module, the output clock rate for the synchronization circuitry matches the clock signal controlling the analog to digital converter.

12. A digital phased array transmitter for transmitting electromagnetic energy, comprising:

a plurality of antenna elements capable of transmitting electromagnetic energy; and

a transmit module coupled to each of the plurality of antenna elements, the transmit module including a digital to analog converter controlled by a clock signal generated by clock circuitry coupled to a delay circuit;

wherein each delay circuit delays a base clock signal from the clock circuitry by a desired amount so that a transmit direction of the plurality of antenna elements may be electronically controlled.

13. The digital phased array transmitter of claim 12, wherein each digital to analog converter has a multiple bit digital value as an input.

14. The digital phased array transmitter of claim 12, wherein each digital to analog converter is a single bit digital value as an input.

15. The digital phased array transmitter of claim 12, further comprising multiple data conversion circuits coupled to provide an output signal to each analog to digital converter at a first clock rate and having an input signal at a second clock rate.

16. The digital phased array transmitter of claim 15, wherein the first clock rate matches the base clock signal and the second clock rate is slower than the first clock rate.

17. The digital phased array transmitter of claim 12, wherein an amount of delay provided by each delay circuit is programmable.

18. The digital phased array transmitter of claim 17, wherein the plurality of antenna elements are grouped into sets of antenna elements and wherein each antenna element within the same set has the same amount of programmed delay.

19. The digital phased array transmitter of claim 12, wherein the electromagnetic energy is radio-frequency energy.

20. The digital phased array transmitter of claim 17, wherein each delay circuit is controlled by a digital word provided by a control register that may be loaded with a desired delay value.

21. The digital phased array transmitter of claim 12, further comprising synchronization circuitry coupled to each digital to analog converter to receive and then output data to the digital to analog converter at an output clock rate.

22. The digital phased array transmitter of claim 21, wherein for each transmit module, the output clock rate for the synchronization circuitry matches the clock signal controlling the digital to analog converter.

23. A digital phased array transmit/receive module, comprising:

an analog to digital converter having an analog input signal representative of received electromagnetic energy;

a digital to analog converter having a digital input signal representative of electromagnetic energy to be transmitted;

clock circuitry having a clock output signal; and

programmable time delay circuitry coupled to the clock output signal to provide a relative delay to the clock output signal, the delayed clock output signal being coupled to the analog to digital converter to control a sampling rate for the analog to digital converter and being coupled to the digital to analog converter to control a operational rate for the digital to analog converter.

24. The digital phased array transmit/receive module of claim 23, wherein the electromagnetic energy is radio frequency energy.

25. The digital phased array transmit/receive module of claim 23, wherein the programmable delay circuitry comprises a first time delay circuit having a clock output for the analog to digital converter and a second time delay circuit having a clock output for the digital to analog converter.

26. The digital phased array transmit/receive module of claim 23, wherein the programmable delay circuitry comprises a single time delay circuit having a single clock output for both the analog to digital converter and the digital to analog converter.

27. The digital phased array transmit/receive module of claim 23, wherein the programmable delay circuitry comprises digitally programmable micro-electromechanical switch (MEMS) phase shifters.

28. The digital phased array transmit/receive module of claim 23, wherein the programmable delay circuitry comprises digitally programmable diode phase shifters.

29. The digital phased array transmit/receive module of claim 23, wherein the programmable delay circuitry comprises digitally programmable field effect transistor (FET) switching devices.

30. A method for receiving electromagnetic energy, comprising:

receiving analog electromagnetic energy with a plurality of antenna elements;

converting analog information from the plurality of antenna elements to digital information utilizing an analog to digital converters associated with the antenna elements; and

controlling each analog to digital converter with a clock signal generated by clock circuitry coupled to a delay circuit so that each delay circuit delays a base clock signal from the clock circuitry by a desired amount so that a receive direction of the plurality of antenna elements may be electronically controlled.

31. The method of claim 30, wherein each analog to digital converter has a multiple bit digital value as an output.

32. The method of claim 30, wherein each analog to digital converter has a single bit digital value as an output.

33. The method of claim 30, wherein an amount of delay provided by each delay circuit is programmable.

34. The method of claim 33, further comprising grouping the plurality of antenna elements into sets of antenna elements and setting the same amount of programmed delay for each antenna element within the same set.

35. The method of claim 34, wherein the electromagnetic energy is radio-frequency energy.

36. A method for transmitting electromagnetic energy, comprising:

converting digital information to analog information utilizing a plurality of digital to analog converters associated with a plurality of antenna elements;

controlling each digital to analog converter with a clock signal generated by clock circuitry coupled to a delay circuit so that each delay circuit delays a base clock signal from the clock circuitry by a desired amount so that a transmit direction of the plurality of antenna elements may be electronically controlled; and

transmitting electromagnetic energy in the transmit direction.

37. The method of claim 36, wherein each digital to analog converter has a multiple bit digital value as an input.

38. The method of claim 36, wherein each digital to analog converter has a single bit digital value as an input.

39. The method of claim 36, wherein an amount of delay provided by each delay circuit is programmable.

40. The method of claim 39, further comprising grouping the plurality of antenna elements into sets of antenna elements and setting the same amount of programmed delay for each antenna element within the same set.

41. The method of claim 40, wherein the electromagnetic energy is radio-frequency energy.